Claims

1. An integrated circuit comprising:

a die having a surface;

a first area of first circuit cells in said die configurable by user defined interconnections from above said surface;

a second area comprising a plurality of sub-circuit cells forming a module having a predefined functionality, wherein said sub-circuit cells include at least one second circuit cell configured such that when said predefined functionality of said module is not used, said second circuit cell is configurable by user defined interconnections from above said surface.

2. The integrated circuit of claim 1, wherein said second circuit cell comprises at least one of a buffer circuit cell, an inverter circuit cell, a flip-flop circuit cell, a latch circuit cell, a multiplexer circuit cell, an exclusive-OR gate circuit cell, an AND gate circuit cell, and an OR gate circuit cell.

3. The integrated circuit of claim 1, wherein said sub-circuit cells comprise a plurality of said second circuit cells.

4. The integrated circuit of claim 3, wherein said plurality of second circuit cells comprises a plurality of different circuit cell types.

5. The integrated circuit of claim 1, wherein each of said first circuit cells comprises an input terminal at said surface and an output terminal at said surface.

6. The integrated circuit of claim 1, wherein said at least one second circuit cell comprises a first input terminal at said surface and a first output terminal at said surface.

7. The integrated circuit of claim 6, further comprising:

at least one layer of conductive interconnections formed on said surface;

wherein said first input terminal is coupled by a respective conductive interconnection in said layer to a stable signal line.

8. The integrated circuit of claim 7, wherein said stable signal line is a stable voltage line.

9. The integrated circuit of claim 8, wherein said stable voltage line is a power rail.

10. The integrated circuit of claim 7, further comprising at least one used sub-circuit cell disposed among said unused circuit cells.

11. The integrated circuit of claim 10, wherein said used sub-circuit cell comprises a second input terminal at said surface and a second output terminal at said surface.

12. The integrated circuit of claim 10, wherein said used sub-circuit cell is configured as a repeater cell in a routing connection across said area.

13. The integrated circuit of claim 12, wherein said routing connection comprises (i) a first interconnection extending in said layer across a first portion of said area to said second input terminal, and (ii) a second interconnection extending in said layer across a second portion of said area from said second output terminal.

14. The integrated circuit of claim 12, wherein said used sub-circuit cell comprises at least one of a buffer cell and an inverter cell.

15. An integrated circuit comprising:

a die having a surface;

a first general purpose area of said die containing general purpose circuit elements configurable by user defined interconnections from above said surface; and

a plurality of second standard circuit areas containing standard sub-circuits more complicated than said general purpose circuit elements and configurable by user defined interconnections from above said surface;

wherein said plurality of second standard circuit areas are distributed across said first general purpose area at multiple locations and provide locally usable resources at said multiple locations in said first general purpose area.

16. The integrated circuit of claim 15, wherein said plurality of second standard circuit areas are distributed in a substantially uniform pattern.

17. The integrated circuit of claim 15, wherein said plurality of second standard circuit areas are distributed according to a repeating pattern.

18. The integrated circuit of claim 15, wherein said plurality of second standard circuit areas comprise a plurality of circuit arrays.

19. The integrated circuit of claim 15, wherein said general purpose circuit elements comprise logic circuits.

20. The integrated circuit of claim 15, wherein said general purpose circuit elements comprise one or more logic gates.

21. The integrated circuit of claim 15, wherein said standard sub-circuits comprise logic circuits.

22. The integrated circuit of claim 15, wherein said standard sub-circuits comprise a first buffer array circuit cell.

23. The integrated circuit of claim 22, wherein said first buffer array circuit cell comprises an array of buffer circuits, wherein (i) each buffer circuit comprises an input terminal and an output terminal, and (ii) adjacent buffer circuits are oppositely orientated.

24. The integrated circuit of claim 22 wherein said standard sub-circuits further comprise a second buffer array circuit cell extending in a different physical direction from said first buffer array circuit cell.

25. The integrated circuit of claim 24, wherein said standard sub-circuits further comprise general purpose logic circuits more complicated than said general purpose circuit elements.

26. The integrated circuit of claim 25, wherein said general purpose logic circuits comprise at least one of:

an individual buffer;

a logic gate different from said general purpose circuit elements;

a multiplexer; and

a flip flop.

27. The integrated circuit of claim 15, further comprising:

at least one layer of conductive interconnections formed on said surface;

wherein (i) said general purpose circuit elements are coupled to said conductive interconnections in said at least one layer, and (ii) said standard sub-circuits are coupled to said conductive interconnections in said at least one layer.

28. A method for designing an integrated circuit element, comprising the steps of:

(a) providing a first area of said integrated circuit element comprising first circuit cells configurable by user defined interconnections above a surface of said integrated circuit element; and

(b) providing a second area of said integrated circuit element comprising a plurality of sub-circuit cells forming a module having a predefined functionality, wherein said sub-circuit cells include at least one second circuit cell configured such that when said predefined functionality of said module is not used, said second circuit cell is configurable by user defined interconnections from above said surface.